

Performance Evaluation of Digital Phase-Locked Loops for Advanced Deep Space Transponders

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The performances of the digital phase-locked loops (DPLL's) for the advanced deep-space transponders (ADT's) are investigated. DPLL's considered in this article are derived from the analog phase-locked loop, which is currently employed by the NASA standard deep space transponder, using S-domain to Z-domain mapping techniques. Three mappings are used to develop digital approximations of the standard deep space analog phase-locked loop, namely the bilinear transformation (BT), impulse invariant transformation (IIT), and step invariant transformation (SIT) techniques. The performance in terms of the closed loop phase and magnitude responses, carrier tracking jitter, and response of the loop to the phase offset (the difference between the incoming phase and reference phase) is evaluated for each digital approximation. Theoretical results of the carrier tracking jitter for command-on and command-off cases are then validated by computer simulation. Both theoretical and computer simulation results show that at high sampling frequency, the DPLL's approximated by all three transformations have the same tracking jitter. However, at low sampling frequency, the digital approximation using BT outperforms the others. The minimum sampling frequency for adequate tracking performance is determined for each digital approximation of the analog loop. In addition, computer simulation shows that the DPLL developed by BT provides faster response to the phase offset than IIT and SIT.

I. Introduction

In recent years, the topic of the digital phase-locked loop (DPLL) has been studied in great detail and well documented in the literature [1-11]. An excellent survey of the work accomplished during 1960-1980 is provided in [1]. The analysis, design, and performance of the DPLL are dealt with in [4-6]. Optimum DPLL and dig-

ital approximation of the analog loop filter are discussed in [7,8]. Currently, most of the work on the DPLL concentrates in these areas, and very little of it focuses on the optimum digital approximation of the analog phase-locked loop (APLL) [8,9]. Aguirre et al. deal only with the design of an optimum loop filter using the impulse invariant transform (IIT) method, minimization method, estimation-prediction technique, and classical control the-

ory approach. The digital loop filters derived by these methods were compared in [8] in terms of stability, gain margin, steady state, and transient performance. On the other hand, [9] focused on the design of the DPLL based on the APLL. Boman [9] considered four different transformations, namely bilinear transformation (BT), IIT, step invariant transformation (SIT), and rotational transformation (RT). The output phase responses of the approximated digital loops using these transformations were evaluated at low sampling rates in the absence of noise and compared. It was found in [9] that for a simple second-order APLL, the phase response of the digital approximation of the APLL using the IIT method exhibits less overshoot and ringing than the others.

The present work is an extension of [8,9,14] to include many other aspects in determining an optimum transformation technique to develop a good digital approximation of a given APLL. The digital approximation is developed by mapping the continuous time S -domain to the discrete time Z -domain. The mapping is accomplished using BT, IIT, SIT, and RT. Because the RT technique is identical to the IIT technique, only three techniques, namely BT, IIT, and SIT, are considered in this article. For each of these mapping techniques, the phase and magnitude responses of the closed-loop transfer function, the response of the loop to the phase offset, the minimum sampling frequency for adequate tracking performance, and the carrier tracking jitter will be evaluated.

The article is divided into five remaining sections. Section II introduces the current command signal format that is received by the deep space transponder along with a simplified model of the APLL for tracking the carrier. Equivalent DPLL's are also described in this section. Detailed recursive implementations of the DPLL's using BT, IIT and SIT are described in Section III. Included in Section III are the plots of the phase and magnitude responses of the closed-loop transfer functions for each digital approximation. Section IV derives the carrier tracking phase jitter for both analog and digital loops with command-on and command-off. Section V presents the computer simulation results to verify the theoretical results obtained in Section IV and to determine the transient response of the digital loops to the initial phase offset. Furthermore, computer simulation results for determining the minimum sampling frequency for each approximation are also presented in Section V. Section VI presents the key conclusions of the article.

II. System Modeling

The mathematical model for the command signal to the spacecraft transponder, $S(t)$, is defined as

$$S(t) = \sqrt{2P} \sin((\omega_C + \omega_d)t + \Theta(t) + \phi) \quad (1)$$

where P denotes the total received power; $\omega_C = 2\pi f_C$ is the angular carrier frequency; ω_d is the Doppler angular frequency offset; $\Theta(t)$ characterizes the phase modulation, and ϕ characterizes the phase offset. The phase modulation employed by the deep space transponder is $\Theta(t) = md(t) \sin(\omega_{SC}t) + m_R R(t)$, where m is the command modulation index; $d(t)$ denotes the command nonreturn-to-zero (NRZ) data; $\omega_{SC} = 2\pi f_{SC}$ is the command angular subcarrier frequency; m_R is the ranging modulation index, and $R(t)$ denotes the ranging signal.

Without loss of generality, we can set $\omega_C = 2\pi F_{IF}$, and $\omega_d = 0$, and $\phi = 0$, and expand Eq. (1) to get

$$S(t) = \sqrt{2P} [\cos(\Theta(t)) \sin(2\pi F_{IF}t) + \sin(\Theta(t)) \cos(2\pi F_{IF}t)] \quad (2)$$

Ignoring the higher-order-harmonic component, it can be shown that the first term in Eq. (2) represents the carrier component, and the second is the command signal component [16]. Presently, the carrier component is tracked by an APLL. Illustrated in Fig. 1 is a simplified block diagram of the analog carrier tracking loop which is currently employed by the NASA standard deep space transponder. The APLL depicted in Fig. 1 is a type I, second-order loop with the following characteristics:

$$AK = \text{loop gain} = 2.4 \times 10^7 \quad (3)$$

$$B(S) = \frac{1}{(1 + \tau_{RC}S)}; \quad \tau_{RC} = 1.6 \times 10^{-5} \text{sec} \quad (4)$$

$$F(S) = \frac{1 + \tau_2 S}{1 + \tau_1 S}; \quad \tau_1 = 4707 \text{ sec}; \quad \tau_2 = 0.0442 \text{ sec} \quad (5)$$

$$V(S) = \frac{1}{(1 + \tau_V S)}; \quad \tau_V = 1.0 \times 10^{-6} \text{ sec} \quad (6)$$

$$K(S) = \frac{1}{S} \quad (7)$$

Note that $B(S)$ is the typical lowpass filter (LPF); $F(S)$ is the loop filter; $V(S)$ is the roll-off filter of the voltage-controlled oscillator (VCO); and $K(S)$ is the VCO integrator. Let $G(S)$ be the transfer function, excluding the ideal integrator $K(S)$, of the analog loop defined as follows:

$$G(S) = B(S)F(S)V(S) \quad (8)$$

Based on the APLL described in Fig. 1, the equivalent digital counterparts are shown in Figs. 2 and 3. Figure 2 shows the first configuration, the so-called configuration I, for the digital approximation of the analog loop. Configuration I is developed using direct transformation of each functional block in the analog loop—i.e., $B(S)$, $F(S)$, $V(S)$, and $K(S)$ —into the Z -domain. In Fig. 2, M stands for the sample rate reduction factor, and NCO stands for numerically controlled oscillator. On the other hand, configuration II, shown in Fig. 3, is developed by transforming $G(S)$ and $K(S)$ into the Z -domain. Notice that the digital approximations of the APLL illustrated in Figs. 2 and 3 have the sum-and-dump circuit to reduce the sample rate by a factor of M before digital filtering. The sample rate is reduced to a rate such that the implementation of the digital filter is feasible using current digital signal processors. In the following section, the recursive implementations of the LPF, VCO roll-off filter, loop filter, VCO integrator, and the transfer function $G(S)$ will be described.

III. Recursive Implementations of $B(S)$, $F(S)$, $V(S)$, $G(S)$, and $K(S)$

To obtain the digital approximation of the analog carrier PLL described in Figs. 2 and 3, each functional block in the analog loop—i.e., $B(S)$, $F(S)$, $V(S)$, and $K(S)$ —can be mapped directly into the Z -domain using BT or the composite function $G(S)$, which uses IIT or SIT. As mentioned earlier, this section will deal only with BT/IIT/SIT, and BT and IIT/SIT correspond to configurations I and II, respectively. Notice that when using the BT technique, one does not map the composite function $G(S)$ because of the mathematical complexity associated with this technique. Moreover, when using the IIT and SIT techniques, one does not map each functional block in the analog loop because one wants to preserve the impulse and step responses of the loop, respectively, at the sampling points.

A. Bilinear Transformation Method

Given a proper sampling frequency, this method preserves the phase characteristics in the narrow passband

when mapping the analog PLL into the digital domain. The mapping from analog (S -domain) to discrete domain (Z -domain) can be achieved by direct substitution of the following equation into the analog transfer function [12–14].

$$S = \frac{2(Z-1)}{T_S(Z+1)} \quad (9)$$

where T_S denotes the sampling period, and $F_S = 1/T_S$ denotes the sampling frequency. To obtain the digital approximation of the analog filters using bilinear transformation, one substitutes Eq. (9) into Eqs. (4), (5), (6), and (7) to get $B(Z)$, loop filter $F(Z)$, $V(Z)$, and $K(Z)$. The results are

$$B(Z) = \frac{(1+Z^{-1})}{(A_{00}Z^{-1} + A_{11})} \quad (10)$$

$$F(Z) = \frac{(A_0Z - B_0)}{(A_1Z - B_1)} \quad (11)$$

$$K(Z) = \frac{T_S(Z+1)}{2(Z-1)} \quad (12)$$

where

$$A_{00} = 1 - C_0; \quad A_{11} = 1 + C_0 \quad (13)$$

$$\left. \begin{aligned} A_0 &= 1 + a_0 \\ A_1 &= 1 + b_0 \\ B_0 &= a_0 - 1 \\ B_1 &= b_0 - 1 > 0 \end{aligned} \right\} \quad (14)$$

and

$$C_0 = \frac{2\tau_{RC}}{T_S}; \quad a_0 = \frac{2\tau_2}{T_S}; \quad b_0 = \frac{2\tau_1}{T_S} \quad (15)$$

Note that the Z -domain representation for $V(S)$ is exactly the same as in Eq. (10) except that C_0 , A_{00} , and A_{11} are replaced by, respectively,

$$C_{01} = \frac{2\tau_V}{T_S}; \quad A_{01} = 1 - C_{01}; \quad A_{10} = 1 + C_{01} \quad (16)$$

The digital closed-loop transfer function, $H(Z)$, for this case is given by

$$H(Z) = \frac{AK [B(Z)F(Z)V(Z)K(Z)]}{1 + AK [B(Z)F(Z)V(Z)K(Z)]} \quad (17)$$

Plots of the analog and digital closed-loop phase and magnitude responses are shown in Figs. 4(a) and 4(b). These figures show that for sampling frequencies below 80 kHz, distortions in phase and magnitude can occur for the digital approximation loop. In addition, the figures show that for sampling frequencies greater than or equal to 80 kHz, the response of the digital loop approaches that of the analog counterpart. Hence, to achieve the same response as the analog loop, the minimum sampling frequency for this case is 80 kHz. Later on, the minimum sampling frequency to achieve acceptable tracking performances will be investigated by computer simulation. Figures 5(a), 5(b), and 5(c) show the recursive implementations of the loop filter $F(Z)$, the integrator $K(Z)$, and the LPF $B(Z)$, respectively.

B. Impulse Invariant Transformation Method

This mapping technique preserves the impulse response at the sampling points. Let $g(t)$ be the impulse response of $G(S)$, i.e., $g(t) = L^{-1}\{G(S)\}$, where $L^{-1}\{\cdot\}$ denotes the inverse Laplace transform of $\{\cdot\}$. Thus, the digital approximation of the analog transfer function $G(S)$ is given by [12–14]

$$G_D(Z) = T_S [z\{g(t)|t = nT_s\}] \quad (18)$$

where $z\{\cdot\}$ is the z -transform of $\{\cdot\}$. Note that the analog transfer function $G(S)$ considered in this article is defined as in Eq. (8). Similarly, one can get the equivalent digital approximation for the integrator $K(S)$. It is found to be

$$K(Z) = \frac{ZT_S}{(Z - 1)} \quad (19)$$

The digital approximation for the analog transfer function $G(S)$, which is given in Eq. (8), is obtained by finding the inverse Laplace transform of $G(S)$ and then substituting the resultant into Eq. (18). Evaluating Eq. (18), one has

$$G_D(Z) =$$

$$T_S \left[\frac{\alpha_0}{1 - Z^{-1}e^{-aT_S}} + \frac{\alpha_1}{1 - Z^{-1}e^{-bT_S}} + \frac{\alpha_2}{1 - Z^{-1}e^{-cT_S}} \right] \quad (20)$$

where

$$\alpha_0 = \frac{\tau_1 - \tau_2}{(\tau_1 - \tau_{RC})(\tau_1 - \tau_V)} \quad (21)$$

$$\alpha_1 = \frac{\tau_{RC} - \tau_2}{(\tau_{RC} - \tau_1)(\tau_{RC} - \tau_V)} \quad (22)$$

$$\alpha_2 = \frac{\tau_V - \tau_2}{(\tau_2 - \tau_1)(\tau_V - \tau_{RC})} \quad (23)$$

and

$$a = \frac{1}{\tau_1}; \quad b = \frac{1}{\tau_{RC}}; \quad c = \frac{1}{\tau_V} \quad (24)$$

The digital closed-loop transfer function for this case is given by

$$H(Z) = \frac{AZ[G_D(Z)K(Z)]}{1 + AK[G_D(Z)K(Z)]} \quad (25)$$

From Eq. (25), the plots of the phase and magnitude responses can be obtained for the digital approximation loop. Figures 6(a) and 6(b) illustrate the closed-loop phase and magnitude responses for both analog and digital loops. The figures show that the response of the digital loop approximated using impulse invariant transformation is the same as that of the analog loop when the sampling frequency is higher than or equal to 80 kHz. When the sampling frequency is less than 80 kHz, the digital loop can encounter serious distortion in both phase and amplitude responses. The recursive implementations $G_D(Z)$ and $K(Z)$ using impulse invariant transformation are shown in Figs. 7(a) and 7(b).

C. Step Invariant Transformation Method

This method preserves the step response at the sampling points when mapping S -domain to Z -domain. The

relationship between the analog and digital transfer function is [12–14]

$$G_D(Z) = \frac{Z-1}{Z} z \left\{ \left[L^{-1} \left[\frac{G(S)}{S} \right] \right]_{t=nT_s} \right\} \quad (26)$$

where $z\{\cdot\}$ and $G(S)$ are defined as they are above. The digital approximation $K(Z)$ for $K(S)$ using step invariant transformation can be obtained in a similar manner. The results are

$$K(Z) = \frac{T_s}{(Z-1)} \quad (27)$$

$$G_D(Z) = \beta_0 + \beta_1 \left[\frac{1-Z^{-1}}{1-Z^{-1}e^{-aT_s}} \right] + \beta_2 \left[\frac{1-Z^{-1}}{1-Z^{-1}e^{-bT_s}} \right] + \beta_3 \left[\frac{1-Z^{-1}}{1-Z^{-1}e^{-cT_s}} \right] \quad (28)$$

where

$$\beta_0 = \frac{\alpha_0}{a} + \frac{\alpha_1}{b} + \frac{\alpha_2}{c} \quad (29)$$

$$\beta_1 = -\frac{\alpha_0}{a}; \quad \beta_2 = -\frac{\alpha_1}{b}; \quad \beta_3 = -\frac{\alpha_2}{c} \quad (30)$$

The parameters α_0 , α_1 , α_2 , a , b , and c are defined in Eqs. (21) through (24). Again, Eq. (25) can be used to evaluate the closed-loop transfer function for this case. The plots of the closed-loop transfer functions for both analog and digital loops are shown in Figs. 8(a) and 8(b). The figures show that the magnitude response approaches the analog response when the sampling frequency is higher than or equal to 100 kHz. However, the phase response suffers serious distortion when the sampling frequency is less than 1 MHz. Thus, in order to achieve the same response as the analog loop, the digital approximation loop using step invariant transformation must be sampled at least at 1 MHz, i.e., this method requires 10 times higher sampling frequency than the previous methods. Table 1 summarizes the results in finding the minimum sampling frequency, F_s , that is required for the digital loop to achieve the same phase and amplitude responses as the analog loop. The recursive implementations of $G_D(Z)$ and $K(Z)$ using step invariant transformation are shown in Figs. 9(a) and 9(b).

IV. Carrier Tracking Performances of the Approximated Digital Loops

The tracking performance of the APLL for high loop signal-to-noise ratio (LSNR) is well known [15,16]. For LSNR > 5 dB, the variance of the tracking phase error is approximated by

$$\sigma_\phi^2 = \frac{N_0 B_L}{P_C} \quad (31)$$

where N_0 is the one-sided thermal noise spectral density, B_L denotes one-sided tracking loop noise bandwidth, and P_C is the carrier power. Note that LSNR = 5 dB is the loop threshold point where the nonlinear theory and linear theory depart severely (by about 1 dB or more in terms of tracking variance). The mathematical expressions for the analog loop bandwidth and carrier power are given by [15,16]

$$2B_L = \frac{1}{2\pi} \int_{-\infty}^{\infty} |H(j\omega)|^2 d\omega \quad (32)$$

where $H(j\omega)$ is the analog closed-loop transfer function, which is identical to Eq. (17) with Z replaced by $s = j\omega$. Using the loop gain, the LPF, the loop filter, the roll-off filter of the VCO, and the VCO integrator given in Eqs. (3) to (7), respectively, the one-sided tracking loop noise bandwidth is calculated using Eq. (32). The result is $B_L = 62$ Hz.

For the digital loops, the one-sided loop noise bandwidth B_{DL} is given by

$$B_{DL} = \frac{1}{4\pi j T_s H^2(1)} \oint_{|Z|=1} H(Z) H(Z^{-1}) \frac{dZ}{Z} \quad (33)$$

where $j = \sqrt{-1}$ and $H(Z)$ is the closed-loop digital transfer function which is given by Eqs. (17) and (25) for BT and IIT/SIT, respectively. The digital loop noise bandwidth for IIT can be calculated by substituting the digital transfer function $G_D(Z)$, shown in Eq. (20), into Eq. (25) and then substituting the resultant into Eq. (33). For SIT, Eq. (26) is used instead of Eq. (20) for the digital transfer function $G_D(Z)$.

In this article, Eq. (32) will be evaluated numerically using an analytical computer program for the three transformation methods under investigation. The numerical results are plotted in Fig. 10. Figure 10 shows a plot B_L/F_s

(or $B_L T_S$) versus B_{DL}/F_S (or $B_{DL} T_S$) for BT, IIT, and SIT. This figure shows that, for $B_L T_S \leq 0.01$, the tracking loop noise bandwidth of the digital approximation of the analog loop using BT is almost identical to that of the analog loop. On the other hand, the digital loop noise bandwidth obtained by using IIT/SIT departs from the analog loop bandwidth when $B_L T_S \geq 0.001$. Notice that SIT provides the worst digital approximation, and BT is the best among the three transformations. Table 2 gives a brief summary of the numerical results shown in Fig. 10.

Figure 10 shows that, for $B_L T_S \leq 0.01$ (corresponding to $F_S \leq 6.2$ kHz), the digital tracking loop bandwidth approximated by BT is the same as the analog loop. Moreover, the loop bandwidths of the digital loops approximated by IIT and SIT are worse than those of the analog counterpart for $B_L T_S \geq 0.001$ (corresponding to $F_S = 62$ kHz). This implies that in order to achieve the same tracking phase error as the analog loop, the digital loop approximated by BT requires lower sampling frequency

than the IIT and SIT loops. For the analog loop with characteristics specified in Section II, it is found that the minimum digital-loop sampling frequency that is required for the digital loop to have the same tracking loop bandwidths as the analog is 6.2 kHz, and this is only achievable through BT. It has been shown in Table 1 that the minimum sampling frequency required to achieve the same phase and amplitude responses as the analog is 80 kHz for both BT and IIT, and 1 MHz for SIT. Hence, what will be the minimum sampling frequency that one would select for optimum performance? The answer to this question will be deferred until Section V.

It should be mentioned that Eq. (33) can also be evaluated analytically by expressing $H(Z)$ in the following form:

$$H(Z) = \frac{b_0 Z^4 + b_1 Z^3 + b_2 Z^2 + b_3 Z^1 + b_4}{a_0 Z^4 + a_1 Z^3 + a_2 Z^2 + a_3 Z^1 + a_4} \quad (34)$$

and then from Table III in [17], Eq. (35) becomes

$$B_{DL} = \left[\frac{1}{2T_S H^2(1)} \right] \left[\frac{a_0 b_0 Q_0 - a_0 B_1 Q_1 + a_0 B_2 Q_2 - a_0 B_3 Q_3 + B_4 Q_4}{a_0 \{ (a_0^2 - a_4^2) Q_0 - (a_0 a_1 - a_3 a_4) Q_1 + (a_0 a_2 - a_2 a_4) Q_2 - (a_0 a_3 - a_1 a_4) Q_3 \}} \right] \quad (35)$$

where

$$B_0 = b_0^2 + b_1^2 + b_2^2 + b_3^2 + b_4^2; \quad B_1 = 2(b_0 b_1 + b_1 b_2 + b_2 b_3 + b_3 b_4) \quad (36)$$

$$B_2 = 2(b_0 b_2 + b_1 b_3 + b_2 b_4); \quad B_3 = 2(b_0 b_3 + b_1 b_4); \quad B_4 = 2b_0 b_4 \quad (37)$$

$$Q_0 = a_0 e_1 e_4 - a_0 a_3 e_2 + a_4 (a_1 e_2 - e_3 e_4); \quad Q_1 = a_0 a_1 e_4 - a_0 a_2 a_3 + a_4 (a_1 a_2 - a_3 e_4) \quad (38)$$

$$Q_2 = a_0 a_1 e_2 - a_0 a_2 e_1 + a_4 (a_2 e_3 - a_3 e_2); \quad Q_3 = a_1 (a_1 e_2 - e_3 e_4) - a_2 (a_1 e_1 - a_3 e_3) + a_3 (e_1 e_4 - a_3 e_2) \quad (39)$$

$$Q_4 = a_0 [e_2 (a_1 a_4 - a_0 a_3) + e_5 (a_0^2 - a_4^2)] + (e_2^2 - e_5^2) [a_1 (a_1 - a_3) + (a_0 - a_4) (e_4 - a_2)] \quad (40)$$

$$e_1 = a_0 + a_2; \quad e_2 = a_1 + a_3; \quad e_3 = a_2 + a_4 \quad (41)$$

$$e_4 = a_0 + a_4; \quad e_5 = a_0 + a_2 + a_4 \quad (42)$$

As an example, for BT, one gets

$$a_0 = 2F_S A_{10} A_{11} + AK A_0; \quad a_1 = 2F_S (A_{10} A_{00} A_1 + A_{01} A_{11} A_1 - A_{10} A_{11} B_1 - A_{11} A_{10} A_1) + AK (3A_0 - B_0) \quad (43)$$

$$a_2 = 2F_S A_1 (A_{00} A_{01} - A_{01} A_{11}) + 2F_S B_1 (A_{10} A_{11} - A_{10} A_{00} - A_{01} A_{11}) + 3AK(A_0 - B_0) \quad (44)$$

$$a_3 = 2F_S B_1 (A_{00} A_{10} - A_{01} A_{00} + A_{01} A_{11}) - 2F_S A_1 A_{01} A_{00} + AK(A_0 - 3B_0); \quad a_4 = 2F_S B_1 A_{10} A_{00} - AK B_0 \quad (45)$$

$$b_0 = AK A_0; \quad b_1 = AK(3A_0 - B_0); \quad b_2 = 3AK(A_0 - 3B_0) \quad (46)$$

$$b_3 = AK(A_0 - 3B_0); \quad b_4 = -AK B_0 \quad (47)$$

Having determined the corresponding digital loop noise bandwidth, one can evaluate the variance of the tracking phase error for the digital approximations of the analog loop using the following formula from Eq. (31):

$$\sigma_\phi^2 = \frac{N B_{DL}}{P_C} \quad (48)$$

where N is the total one-sided noise spectral density.

When the command and ranging are turned off, i.e., $m = m_R = 0$, all power is allocated to the carrier and there is no interference from the command and ranging to the carrier tracking loop, and hence $N = N_0$. When the command (or ranging) is turned on, there exists some interference between the carrier and the command (or ranging). Since the ranging tones will be placed farther away from the carrier and the power allocated to the ranging is always smaller than the power allocated to the command, the effects of ranging to the carrier tracking loop are negligible and will not be considered here. However, the effects of the command to the carrier tracking may not be neglected because of the increase in the command data rate. Recently, the international Consultative Committee for Space Data Systems (CCSDS) has considered increasing the maximum command data rate from 2 kbits/sec to 4 kbits/sec and the possibility of using a 32-kHz subcarrier frequency for both 2 kbits/sec and 4 kbits/sec.

To determine the effect of interference of the command on the carrier tracking loop, a model of the command data must be provided. Here it is assumed that the command data symbols are equally likely to be +1's and -1's and that successive symbols are uncorrelated. This assumption leads to the power spectral density (PDS) of a unit power sinusoidal wave subcarrier phase-reversal-keyed by the command data stream. See Eq. (1) for the signal; the PSD is given by [18]

$$S_{CD}(f, T_S, f_{SC}) =$$

$$\sum_{n=2, n=\text{even}}^{\infty} J_n^2(m) [\delta(f - n f_{SC}) + \delta(f + n f_{SC})] + \sum_{k=1, k=\text{odd}}^{\infty} J_k^2(m) [S_D(f - k f_{SC}) + S_D(f + k f_{SC})] \quad (49)$$

where

$$S_D(f) = T_S \left[\frac{\sin(\pi f T)}{\pi f T} \right]^2 \quad (50)$$

where T is the command symbol period. Note that the PSD shown above is evaluated at the carrier frequency. Hence, when the command is on, the total noise spectral density, N , seen by the carrier tracking loop can be approximated using the following relationship:

$$N = N_0 \left[1 + \frac{P_C}{N_0} S_{CD}(B_{DL}, T, f_{SC}) \right] \quad (51)$$

where the definition of P_C , taken from Eq. (1) and [16,18], is

$$P_C = (P) J_0^2(m) \quad (52)$$

where $J_0(\cdot)$ is the zero-order Bessel function. Figure 11 shows the theoretical results obtained for the variance of the carrier tracking phase jitter, σ^2 , as a function of the received signal-to-noise spectral density ratio (SNR), which is P/N_0 , for both analog and digital loops when the command is on. The results were plotted for the modulation index $m = 70$ deg, command subcarrier frequency $f_{SC} =$

32 kHz, command data rate $R_S = 2$ kbits/sec, and sampling frequency $F_S = 1$ MHz. As expected, for high sampling frequency, the tracking jitter of the digital loop using BT/IIT/SIT approaches that of the analog loop. Figure 12 presents the numerical results for the digital loop using BT with both command-on and command-off. The theoretical results shown in this figure will be verified by computer simulations discussed in Section V. Note that the relationship between the total received SNR, P/N_0 , and the carrier tracking loop signal-to-thermal noise spectral density ratio, P_C/N_0 , can be evaluated from Eq. (52), and the results are plotted in Fig. 13.

V. Computer Simulation Results

The digital PPL's shown in Figs. 2 and 3 have been implemented using the Signal Processing Workstation (SPW) of Comdisco, Inc. Simulations have been run to verify the carrier tracking jitter obtained in Section IV and to determine the time responses of the digital loops due to the phase offset between the incoming and the NCO reference phase. The update rate of the loop has been set to be the same as the sampling rate. This is done in the simulation by setting the parameter $M = 1$ (see Figs. 2 and 3). In addition, the simulations have been performed to determine the minimum achievable sampling frequency for each digital approximation.

A. Measurements of the Tracking Jitter and Time Response of the Digital Loops

Computer simulations for the digital loops approximated by BT (see Fig. 2) and IIT/SIT (see Fig. 3) have been run for both command-on (with modulation index set at 70 deg, command data rate of 2 kbits/sec, and subcarrier frequency of 32 kHz) and command-off at 1-MHz sampling frequency. The simulations were run for 2.5 million iterations, and the variance of the carrier phase jitter was measured for four different noise seeds. Table 3 presents the average results of four noise seeds. For the sake of comparison, the results are also plotted in Fig. 12. On the other hand, Fig. 14 shows the simulation results of the digital loops approximated by IIT and SIT at 1 MHz sampling frequency. The simulation results, for all cases at 1-MHz sampling frequency, are in good agreement with the theoretical results.

Computer simulation has been performed to determine the time responses of the digital approximations of the loops using the three transformation techniques described in Section III. A phase offset of $\pi/9$ rad between the incoming phase of the signal and the reference NCO has

been injected into the loop with a 1-MHz sampling rate, and the settling time, t_5 , of each loop to the phase offset was measured. Here, the settling time is defined as the time it takes the loop to catch up with the phase offset, or the time it takes the loop to stabilize in the presence of the phase offset. The results are summarized in Table 4 for the command-off and noise-free cases.

B. Minimum Achievable Sampling Frequency

As shown in Fig. 10 and Table 2, for the analog PLL characteristics specified in Section II, the minimum sampling frequencies required for the digital loop to achieve the same analog tracking loop bandwidth are 6.2 kHz and 62 kHz for BT and for IIT/SIT, respectively. On the other hand, it has been shown in Section III that the minimum sampling frequencies required for the digital loop to have the same closed-loop phase and amplitude responses are 80 kHz and 1 MHz for BT/IIT and SIT, respectively. Based on these results, one is tempted to select the smallest sampling frequency so that the requirements on the speed of the digital signal processor and power consumption can be minimized. However, the selected sampling frequencies (based on these criteria) may not be able to provide the required tracking performance. Computer simulation will be used as an additional tool to assist in deciding the minimum achievable sampling frequency. Here, the minimum achievable sampling frequency, denoted as F_{Sm} , is defined as the frequency that satisfies the tracking performance requirement. Table 5 summarizes the simulation results for a 200-kHz carrier frequency, 32-kHz subcarrier frequency, data rate of 2 kbits/sec, modulation index of 70 deg, and P/N_0 of 35 dB-Hz.

The phase jitters shown in Table 5 are then compared with the analog phase jitter of 0.045 rad^2 for this particular case—Eq. (50) with B_{DL} replaced by $B_L = 62 \text{ Hz}$. It is observed that the variance of the tracking phase error, σ_ϕ^2 , of the digital loop approximated by BT is as good as that of the analog loop when the sampling frequency is about 24.8 kHz. Moreover, the tracking phase errors of the digital loops approximated by IIT and SIT are close to those of the analog loop when the sampling frequencies are 240 kHz and 1000 kHz, respectively. The results for the minimum achievable sampling frequency (or optimum sampling frequency) for the three transformations, shown in Table 5, are then compared to the results obtained in Sections III and IV. Recall that Section III determines the minimum sampling frequency, denoted as F_{Smb} , that is required for the digital loops to achieve the same amplitude and phase responses as the analog loop, and that Section III calculates the minimum sampling frequency, denoted as F_{Smb} , for the digital loops to have the same tracking loop

bandwidth as the analog loop. Table 6 summarizes the final results regarding the optimum sampling frequency that is required for each digital approximation method. Table 6 shows that the minimum achievable sampling frequency for both BT and IIT is about four times F_{Smb} and, for SIT, the minimum achievable sampling frequency is the same as F_{Smr} .

VI. Conclusion

Digital approximations of the current analog deep space carrier tracking loop have been investigated in detail. The performance of each approximation was determined for the closed-loop phase and magnitude responses, carrier tracking jitter, response of the loop to the phase offset, and minimum achievable sampling frequency. The numerical results show that BT appears to give the best performance at a low sampling rate, i.e., about $100 B_L$, as compared to the other transformations. The best performance at a low sampling frequency is evident from the closed-loop phase and magnitude response curves, the carrier tracking loop bandwidth curves, and the computer simulation results for the tracking phase error. However, at a high sampling frequency (higher than or equal to 1 MHz, for the case considered in this article), the performance of the DPLL approximated by all three transformations approaches that of the analog loop. It was found that in order to achieve the same tracking phase error as the analog loop, the minimum sampling frequencies required for

BT/IIT and SIT are $4 F_{Smb}$ and F_{Smr} , respectively. Here, F_{Smb} and F_{Smr} denote the minimum sampling frequencies for the digital loops to have the same tracking loop bandwidth and phase/magnitude responses, respectively, as the analog loop. In addition, using the particular analog loop considered in this article, the simulation results show that the response to the incoming phase offset of $\pi/9$ rad of the digital loop approximated by BT is faster than that of the loops approximated by IIT and SIT by about 20 and 30 msec, respectively.

As pointed out in [9], in the absence of noise, the digital loop approximated by the IIT method exhibits less overshoot and ringing in the output response than the others. However, this may not be the key criterion in the selection of the optimum transformation method for approximating the analog loop. This article has shown that, for applications that require low sampling frequency, the BT method appears to give the best performance in terms of the tracking phase error and response to the initial phase offset. Therefore, when the key requirements, such as low sampling rate, low tracking phase error, and fast response to the initial phase offset, for approximating the analog loop are desired, then the BT method is recommended. Furthermore, the performance evaluation approach presented in this article can easily be extended to (1) find the minimum achievable sampling frequency required to approximate any analog loop, and (2) determine the tracking phase error of the digital approximation of the analog loop.

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Table 1. Minimum sampling frequency, F_S , required for the digital approximation to achieve the same phase and amplitude responses as the analog loop.

Transformation method	Minimum F_S required, kHz
Bilinear	80
Impulse invariant	80
Step invariant	1000

Table 2. Loop noise bandwidth of the digital approximations for $F_S = 6.2$ kHz and 62 kHz.

Transformation method	Analog loop noise bandwidth, B_L , Hz	Digital loop noise bandwidth, B_{DL} , at $F_S = 6.2$ kHz, Hz	Digital loop noise bandwidth, B_{DL} , at $F_S = 62$ kHz, Hz
Bilinear	62	62	62
Impulse invariant	62	76.88	62
Step invariant	62	114.08	62

Table 3. Simulation results for command-on (with $m = 70$ deg, $f_{SC} = 32$ kHz, and $R_S = 2$ kbits/sec), and command-off at 1-MHz sampling frequency.

P/N_0 , dB-Hz	Variance of the carrier phase jitter, rad ²					
	Command-off			Command-on		
	BT	IIT	SIT	BT	IIT	SIT
30	0.064000	0.062250	0.063800	0.151000	0.150750	0.150250
35	0.019670	0.019175	0.019400	0.045100	0.044725	0.045250
40	0.006165	0.006013	0.006040	0.014000	0.013875	0.013875
45	0.001945	0.001895	0.001900	0.004398	0.004360	0.004355
50	0.000613	0.000598	0.000598	0.001390	0.001377	0.001378
55	0.000194	0.000189	0.000189	0.000441	0.000435	0.000445
60	6.145×10^{-5}	5.973×10^{-5}	5.960×10^{-5}	0.000139	0.000140	0.000140
65	6.955×10^{-5}	1.818×10^{-5}	1.890×10^{-5}	4.66×10^{-5}	4.623×10^{-5}	4.623×10^{-5}

Table 4. Settling time, t_S , for the phase offset of $\pi/9$ rad.

Transformation method	Settling time, t_S , sec
Bilinear	0.12
Impulse invariant	0.14
Step invariant	0.15

Table 5. Tracking phase jitter as a function of sampling frequency.

F_S , kHz	σ_ϕ^2 , rad ²		
	BT	IIT	SIT
16.5	0.0725	Out of lock	Out of lock
18.5	0.0489	Out of lock	Out of lock
24.8	0.0476	Out of lock	Out of lock
240	0.0453	0.0458	Out of lock
1000	0.0451	0.0447	0.0453

Table 6. Minimum achievable sampling frequency for each transformation method.

Transformation method	Minimum sampling frequency required to achieve the same phase/amplitude responses, F_{Smr} , kHz	Minimum sampling frequency required to achieve the same analog loop bandwidth, F_{Smb} , kHz	Minimum achievable sampling frequency for a specified tracking jitter, F_{Sm} , kHz	Remarks
BT	80	6.20	24.8	$F_{Sm} = 4 F_{Smb}$
IIT	80	62.0	240	$F_{Sm} = 3.9 F_{Smb}$
SIT	1000	62.0	1000	$F_{Sm} = F_{Smr}$

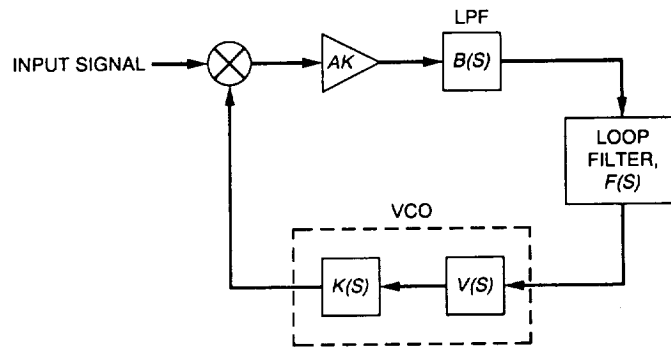


Fig. 1. Simplified block diagram of the analog PLL.

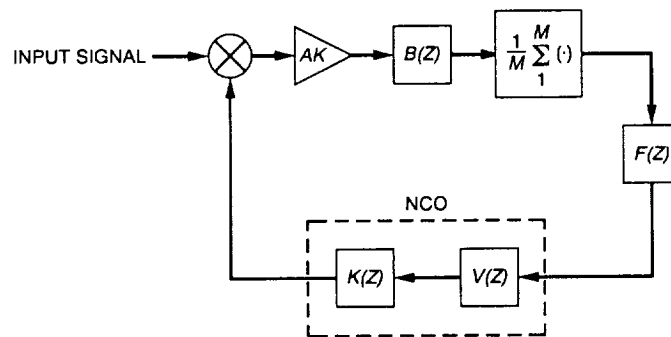


Fig. 2. Digital approximation of the analog PLL—configuration I.

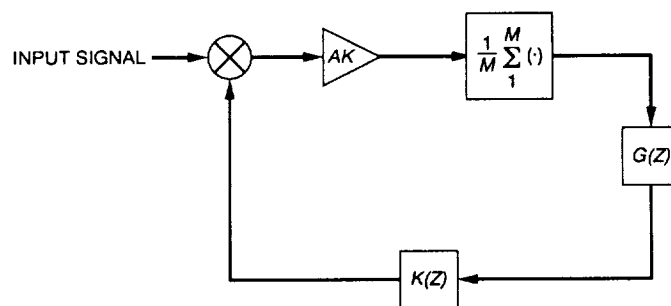


Fig. 3. Digital approximation of the analog PLL—configuration II.

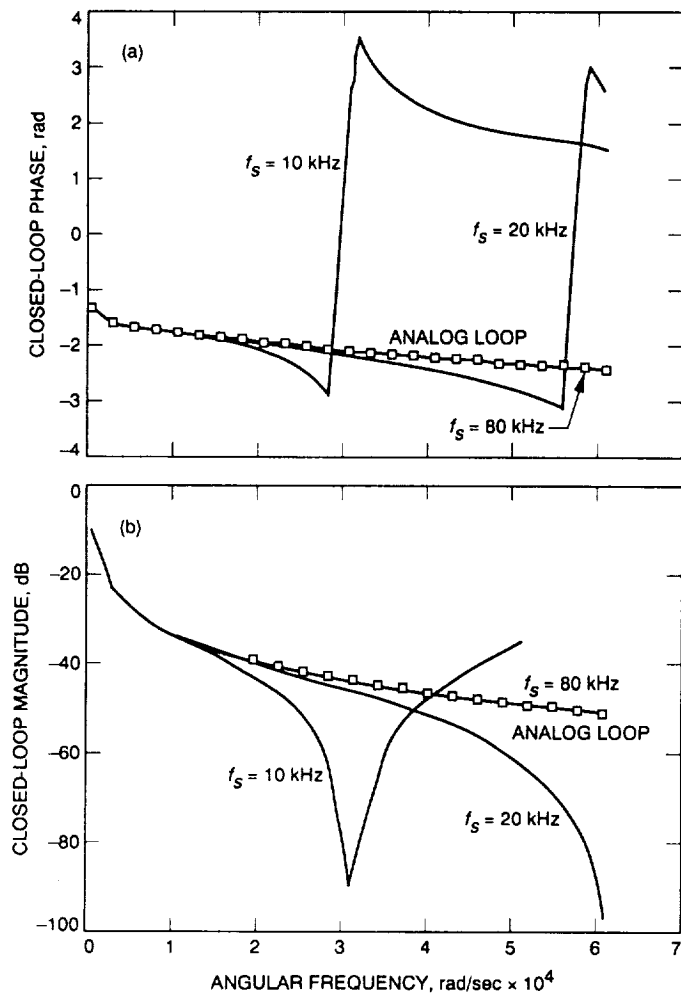


Fig. 4. Closed-loop response of digital approximation using the bilinear transformation method: (a) closed-loop phase characteristics and (b) closed-loop magnitude response.

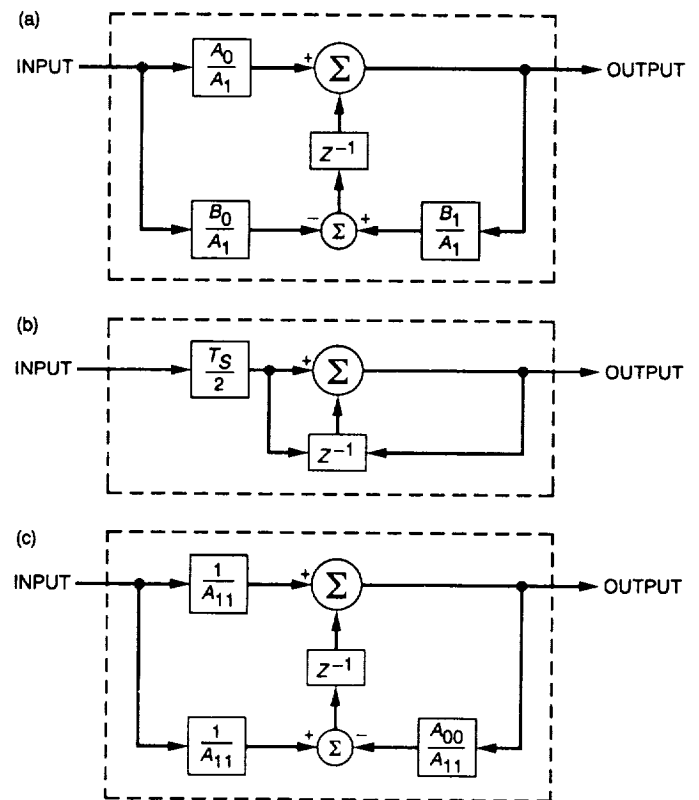


Fig. 5. Recursive Implementation of (a) the loop filter $F(Z)$ (b) the integrator $K(Z)$ and (c) the lowpass filter $B(Z)$ using bilinear transformation.

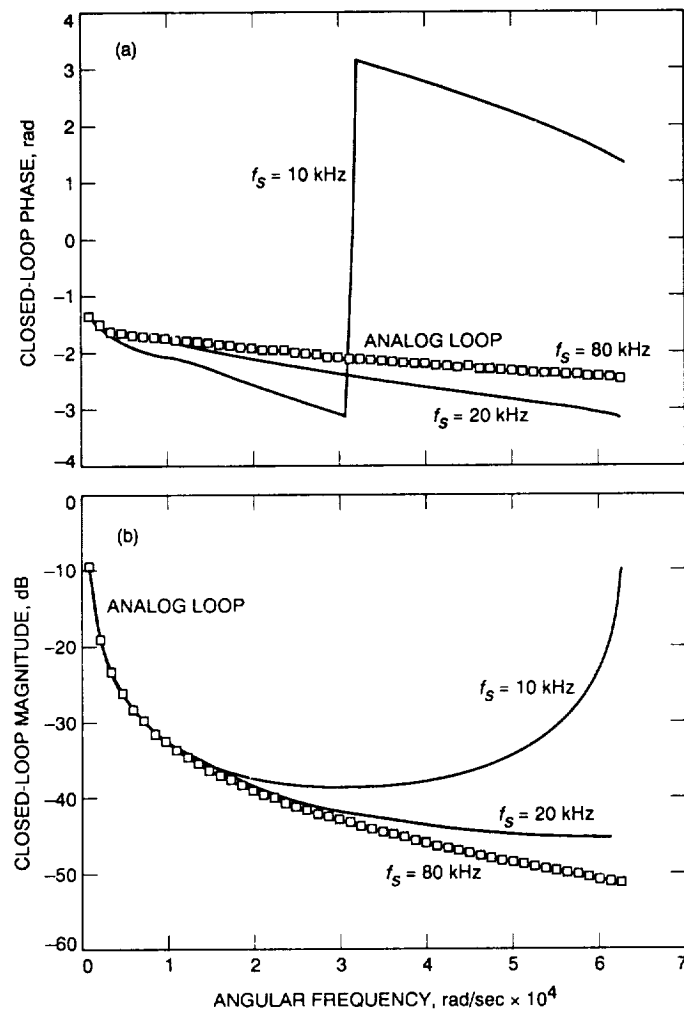


Fig. 6. Closed-loop response of digital approximation using the impulse invariant transformation method: (a) closed-loop phase characteristics and (b) closed-loop magnitude response.

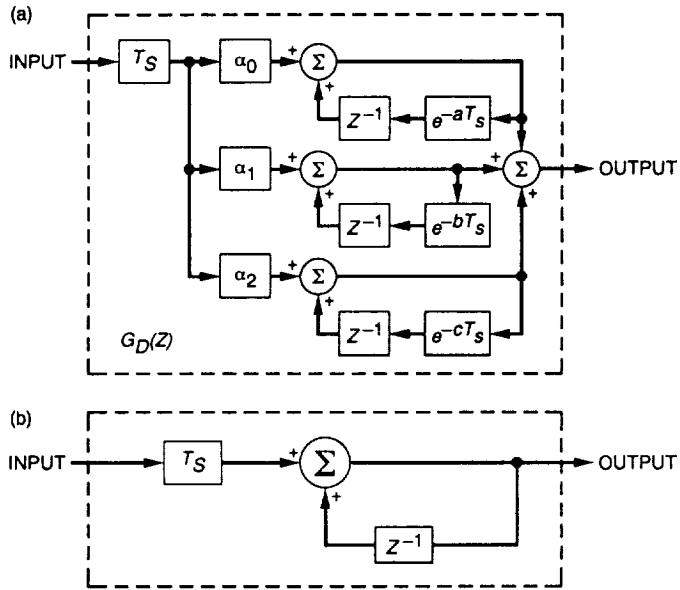


Fig. 7. Recursive Implementation of (a) the open-loop transfer function $G_D(Z)$ and (b) the Integrator $K(Z)$ using Impulse Invariant transformation.

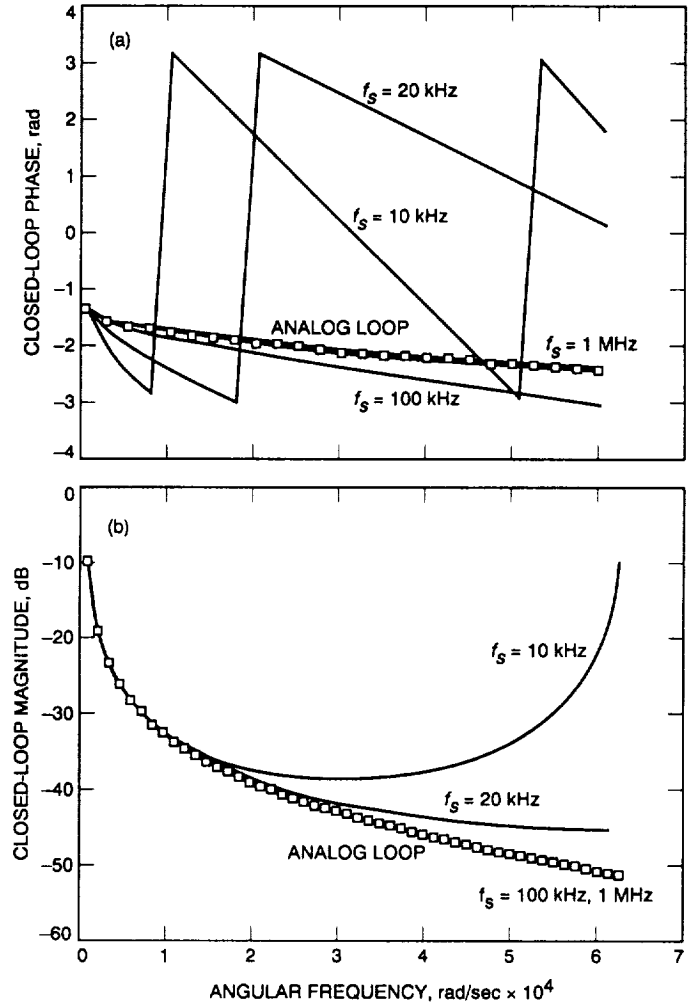


Fig. 8. Closed-loop response of digital approximation using the step invariant transformation method: (a) closed-loop phase characteristics and (b) closed-loop magnitude response.

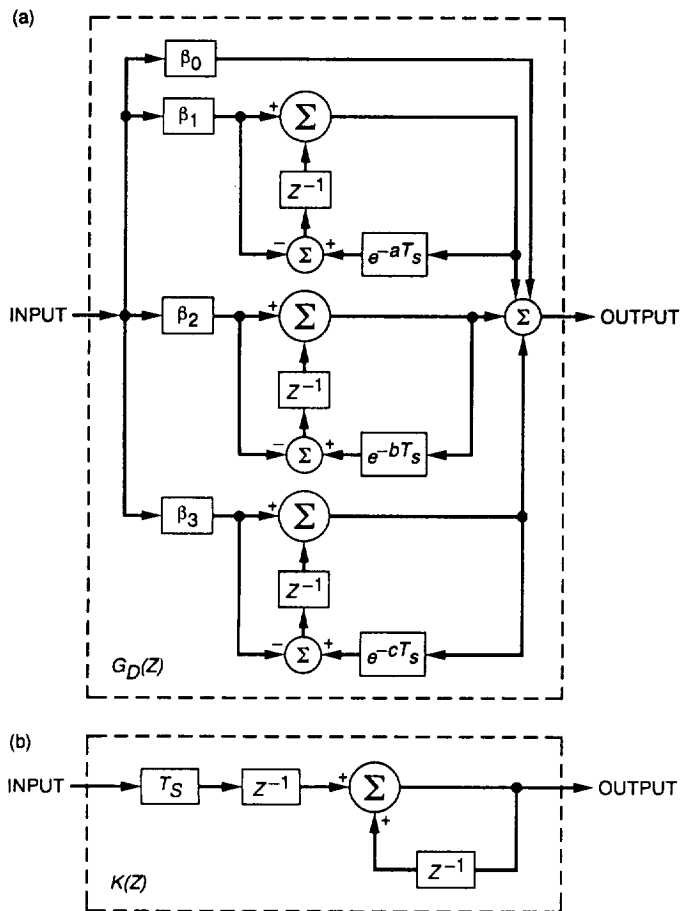


Fig. 9. Recursive Implementation of (a) the open-loop transfer function $G_D(Z)$ and (b) the Integrator $K(Z)$ using step invariant transformation.

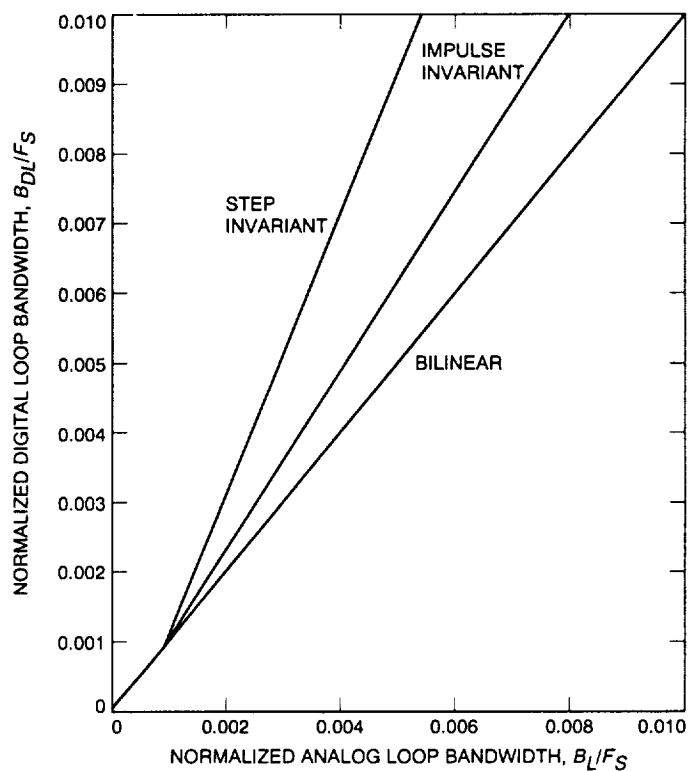


Fig. 10. One-sided digital loop bandwidth for three transformation methods.

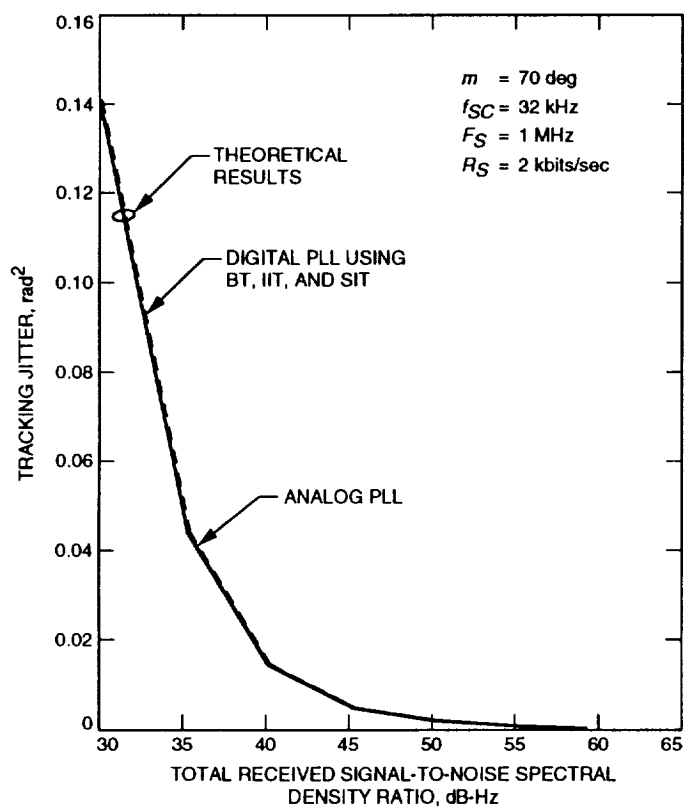


Fig. 11. Theoretical comparison of tracking jitter for analog and digital loops for command-on.

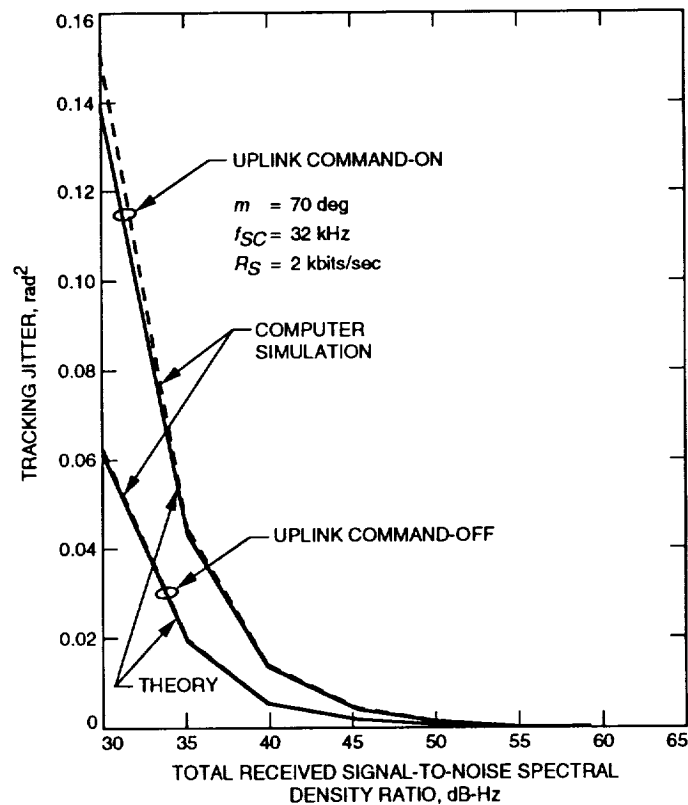


Fig. 12. Tracking phase jitter for the digital loop using bilinear transformation.

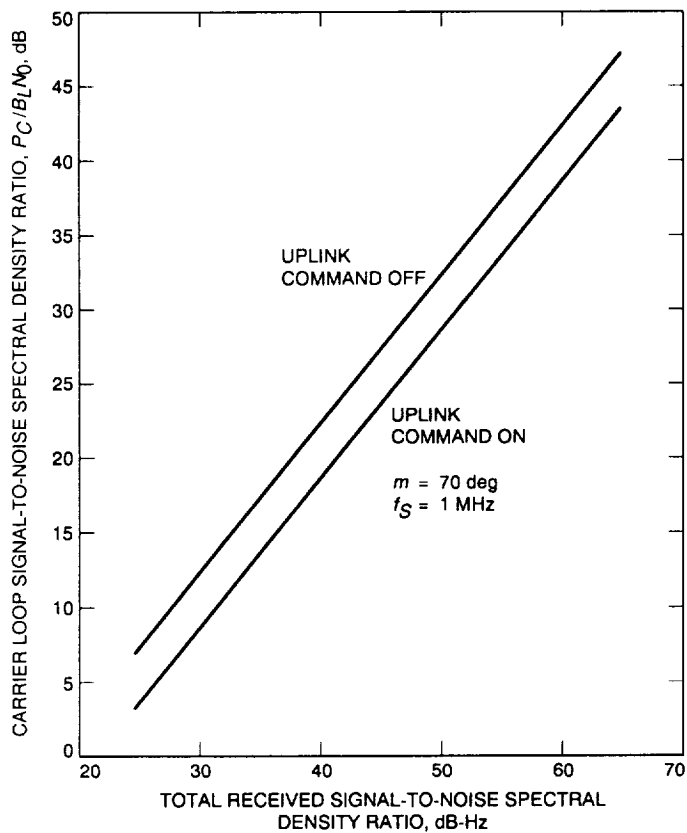


Fig. 13. Carrier loop received signal-to-noise spectral density ratio versus total received signal-to-noise spectral density ratio.

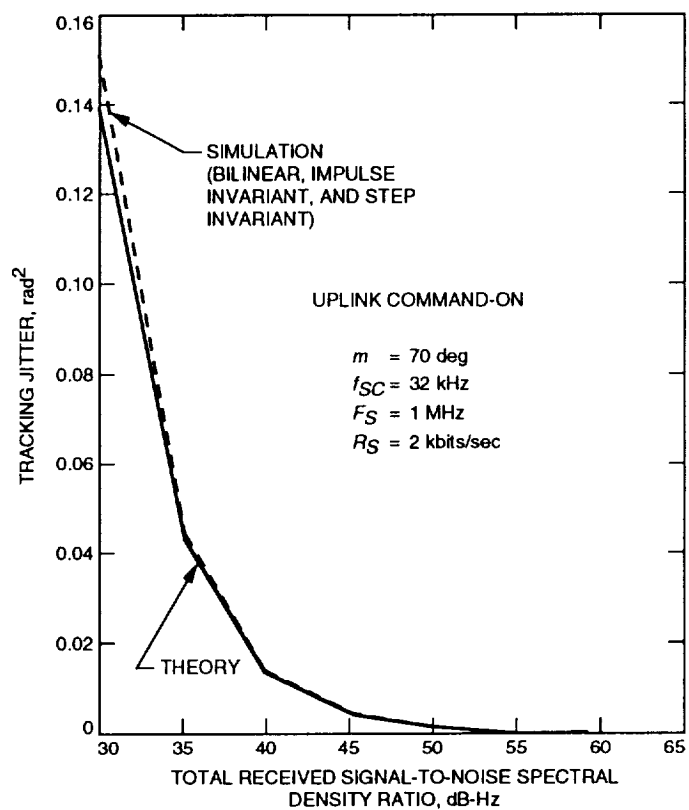


Fig. 14. Comparison of theoretical and simulated tracking phase jitter.

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The Development and Application of Composite Complexity Models and a Relative Complexity Metric in a Software Maintenance Environment

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A great deal of effort is now being devoted to the study, analysis, prediction, and minimization of software maintenance expected cost, long before software is delivered to users or customers. It has been estimated that, on the average, the effort spent on software maintenance is as costly as the effort spent on all other software costs. Software design methods should be the starting point to aid in alleviating the problems of software maintenance complexity and high costs. Two aspects of maintenance deserve attention: (1) protocols for locating and rectifying defects, and for ensuring that no new defects are introduced in the development phase of the software process, and (2) protocols for modification, enhancement, and upgrading. This article focuses primarily on the second aspect, the development of protocols to help increase the quality and reduce the costs associated with modifications, enhancements, and upgrades of existing software. This study developed parsimonious models and a relative complexity metric for complexity measurement of software that were used to rank the modules in the system relative to one another. Some success was achieved in using the models and the relative metric to identify maintenance-prone modules.

I. Introduction

A. Project Objectives

The primary objective of this study was to determine whether software metrics could help guide our efforts in the development and maintenance of the real-time embedded systems that we develop for NASA's Deep Space Net-

work (DSN). Generally, the systems that are developed control receivers, transmitters, exciters, and signal paths through the communication hardware. The most common programming language in our systems is PL/M for Intel 8080, 8086, and 80286 microprocessors; and the systems range in size from 20,000 to 100,000 non-commented lines of code (NCLOC). Approximately 65 percent of the fund-